

# MSP430F41x Device Erratasheet

## Current Version

Devices	Rev:	CPU4	FLL3	PORT3	TA12	TA16	WDG2	XOSC7
MSP430F412	C	✓	✓	✓	✓	✓	✓	✓
MSP430F413	C	✓	✓	✓	✓	✓	✓	✓
MSP430F415	E	✓	✓	✓	✓	✓	✓	✓
MSP430F417	E	✓	✓	✓	✓	✓	✓	✓

Note: See Appendix for prior revisions

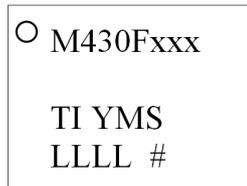
## Package Markings

### PM64: LQFP (PM) 64-pin



YM = Year and Month Date Code  
 LLLL = LOT Trace Code  
 S = Assembly Site Code  
 # = DIE Revision  
 o = PIN 1

### RTD64: QFN (RTD) 64-pin



TI = TI  
 YM = Year and Month Date Code  
 LLLL = LOT Trace Code  
 S = Assembly Site Code  
 # = DIE Revision  
 o = PIN 1

## Detailed Bug Description

### **CPU4** CPU4 - Bug description:

Module: CPU, Function: PUSH #4, PUSH #8

The single operand instruction PUSH cannot use the internal constants (CG) 4 and 8. The other internal constants (0, 1, 2, -1) can be used. The number of clock cycles is different:  
PUSH #CG uses address mode 00, requiring 3 cycles, 1 word instruction  
PUSH #4/#8 uses address mode 11, requiring 5 cycles, 2 word instruction

Workaround implemented in assembler.  
No fix planned.

### **FLL3** FLL3 - Bug description:

Module: FLL+, Function: FLLDx = 11 for /8 may generate an unstable MCLK frequency

When setting the FLL to higher frequencies using FLLDx = 11 (/8) the output frequency of the FLL may have a larger frequency variation (e.g., averaged over 2 seconds) and a lower average output frequency than expected when compared to the other FLLDx bit settings.

Workaround:  
None

### **PORT3** Port3 - Bug description:

Module: PORT1/2, Function: Port interrupts can get lost

Port interrupts can get lost if they occur during CPU access of the P1IFG and P2IFG registers.

Workaround:  
None

### **TA12** TA12 - Bug description:

Module: Timer\_A, Function: Interrupt is lost (slow ACLK)

Timer\_A counter is running with slow clock (external TACLK or ACLK) compared to MCLK. The compare mode is selected for the capture/compare channel and the CCRx register is incremented by 1 with the occurring compare interrupt (if TAR = CCRx).

Due to the fast MCLK the CCRx register increment (CCRx = CCRx+1) happens before the Timer\_A counter has incremented again. Therefore, the next compare interrupt should happen at once with the next Timer\_A counter increment (if TAR = CCRx + 1). This interrupt is lost.

Workaround:  
Switch capture/compare mode to capture mode before the CCRx register increment. Switch back to compare mode afterwards.

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## Detailed Bug Description (continued)

**TA16** TA16 - Bug description:

Module: Timer\_A, Function: First increment of TAR erroneous when IDx > 00

The first increment of TAR after any timer clear event (POR/TACLR) happens immediately following the first positive edge of the selected clock source (INCLK, SMCLK, ACLK, or TACLK). This is independent of the clock input divider settings (ID0, ID1). All following TAR increments are performed correctly with the selected IDx settings.

Workaround:  
None

**WDG2** WDG2 - Bug description:

If a key violation is caused by incorrectly accessing a flash control register, the watchdog interrupt flag is set in addition to a correctly generated PUC.

Workaround:  
None

**XOSC7** XOSC7 - Bug description:

Module: LFXT1 OSC: Oscillation failure in LF mode at low temperatures

When using LFXT1 in LF mode along with the built-in crystal load capacitors, the resulting oscillation duty cycle may decrease, potentially to the point of no oscillation, under operating temperatures less than  $-10^{\circ}\text{C}$ .

Workaround:  
Disable the internal crystal load capacitance (XCAPxPF = 00) and use external load capacitors on XIN and XOUT as recommended by the crystal manufacturer.

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## Appendix: Prior Versions

Devices	Rev:	CPU4	FLL3	PORT3	TA12	TA16	WDG2	XOSC7
MSP430F412	C	✓	✓	✓	✓	✓	✓	✓
MSP430F413	C	✓	✓	✓	✓	✓	✓	✓
MSP430F415	E	✓	✓		✓	✓	✓	
	D	✓	✓		✓	✓	✓	
MSP430F417	E	✓	✓		✓	✓	✓	
	D	✓	✓		✓	✓	✓	

### Detailed Bug Description

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